(2½ Hours) **[Total Marks: 75**

N. B.: (1) **All** questions are **compulsory**.
(2) Make **suitable assumptions** wherever necessary and **state the assumptions** made.
(3) Answers to the **same question** must be **written together**.
(4) Numbers to the **right** indicate **marks**.
(5) Draw **neat labeled diagrams** wherever **necessary**.
(6) Use of **Non-programmable** calculators is **allowed**.

1. Attempt *any three* of the following:

a. What is analog signal? Explain frequency, amplitude with respect to analog signal.

Define analog signal ---- 1M
Draw wave form of it --- 1M
Define frequency with formula f=1/t --- - 2M
Define amplitude --- 1M

b. Encode the following decimal number in binary number system.
i)25.45 3M

divide by 2 method for number 25 and multiply by 2 method for number .45
answer = **11001.011**

ii)134 2M
divide by 2 method
answer= **10000110**

c. Express the 10101100 BCD code into Grey code and also in Excess-3 code.
Ans: This is not a valid BCD number. 5M
Any other answer: 0M

d. i) Perform the subtraction using 1's complement method.
11011 – 10100 3M
Find 1's complement of 10100= 01011
Add with 11011 + 01011=100111
Add carry
Ans= **00111**

ii) Perform the addition of given binary numbers. 2M
1000011 + 1110001
Ans= **10110100**

e. Write a short note on HOLLERITH code. 5M

f. i) Convert 45 octal number into decimal.
Multiply by 8 method 1M
Ans= **37**

ii) Convert 9A hexadecimal number into decimal. 1M

Mulptiply by 16 method
Ans= **154**

2. Attempt *any three* of the following: 15

a. For the logic expression Y=AB'+A'B. Obtain the truth table, name the gate and operation performed and symbol for it also realize this using AND,OR,NOT gates.

Write truth table of Ex –OR gate 1M
Name = Ex-oR gate 1M
Draw symbol of it 1M
Draw the circuit diagram using NOT ,AND and OR gate only 2M

b. Prove the given Boolean expression using Boolean theorem and draw the circuit for it using NAND gate only.
A.B +A'B + A'B' = A' + B

Use theorem associative law 2M
A+A'=1
A+A'B=A+B

Draw the diagram using NAND Gate only
Output of each gate should be written 3M

c. State and prove De-Morgan's theorem and realize it using basic gates.

(A+B)'= A' . B'
(A.B)' = A' +B'
Prove the both theorem with the help of truth table 3M
Draw the diagram using basic gates for both laws 2M

d. Realize the given Boolean expression using NOR gate only.
Y= (A'+B+C) . (A+B'+C') . (A'+B'+C') .(A'+B+C')

Reduce the equation using POS k map method with 3 variable 3M
Answer = (A'+B) . (B'+C')
Draw the circuit diagram using NOR gate only. 2M

e. Using karnaugh's map simplify the following SOP function and implement it with basic gate. F(A,B,C,D) = (2,3,6,7,8,10,11,12) +d(14,15)

Reduce the equation using SOP k map method with 4 variable with 3M
Don't care condition.
Answer = C + AC'D'
Draw the diagram using AND ,NOT and OR gate. 2M

f. Obtain product of sum expression for the following function and implement it using NOR network. F(P,Q,R,S) = (1,3,4,5,6,7,12,13)

Reduce the equation using POS k map method with 4 variable 3M

Answer = (P'+Q'+S).(P'+Q).(Q+R')
Draw the diagram using NOR – NOR network 2M
Write the out put of each gate.

3. Attempt *any three* of the following: 15

a. What is full adder? Draw logic circuit diagram and explain it.

Define full adder 1M
Write the truth table with 3 input, sum and carry. 1M
Circuit diagram 2M
Working of circuit 1M

b. Design BCD to Excess -3 code converter.

Define BCD to Excess-3 code 2M
Circuit diagram 1M
Working of circuit 1M

c. With the help of IC 7483 block diagram explain BCD adder.

Draw block diagram of IC 7483 3M
Explain how this circuit can be used as BCD adder. 2M

d. Describe Half subtractor with help of circuit diagram and truth table.

Define half subtractor 1M
Draw circuit diagram 2M
Write truth table with two inputs and difference and borrow.
Explain working with truth table 2M

e. What is comparator circuit? Discuss detail working of it.

Explain comparator 1M
Draw circuit diagram 2M
Explain working 2M

f. Design and implement Binary to Grey code converter circuit.

Give Binay to grey table 1M
Reduce k map 2M
Design circuit 2M

4. Attempt *any three* of the following: 15

a Draw logic circuit diagram of D flip flop and explain working of it.

Explain D flip flop 1M
Draw circuit diagram 2M
Describe working with different conditions of input 2M

b Discuss clocked S-R flip flop using four NAND gates.

Explain clocked S R flip flop 1M
Draw circuit diagram with 4 NAND gates. 2M
Describe working with different conditions of input explain truth table. 2M

c How JK flip flop is derived from S-R flip flop give the details about it.

Explain how S-R flip flop is derived 1M
S=J.Q'
R=K.Q
Draw circuit diagram 2M
Truth table and explain 2M

d Write a short note on Multiplexer. 1M
Define
Concept and explain 2M
Diagram 2M

e With the help of two 4:1 multiplexer how can we build 8:1 multiplexer? 5M

Diagram and explain

f Explain the roll of ALU as a part of computer system. 5M

Diagram and explain

5. Attempt *any three* of the following: 15

a. Explain the operation of SIPO shift register.

Explain serial in parallel out operation 5M
Circuit diagram and working

b. Discuss Decade counter with help of circuit diagram.

A *decade counter* is one that goes through 10 unique output combinations and then resets as the clock proceeds further. Since it is an MOD-10 counter, it can be constructed with a minimum of four flip-flops. A four-bit counter would have 16 states. By skipping any of the six states by using some kind of feedback or some kind of additional logic, we can convert a normal four-bit binary counter into a decade counter. A decade counter does not necessarily count from 0000 to 1001. It could even count as 0000, 0001, 0010, 0101, 0110, 1001, 1010, 1100, 1101, 1111, 0000, _ _ _ In this count sequence, we have skipped 0011, 0100, 0111, 1000, 1011 and 1110.

A *BCD counter* is a special case of a decade counter in which the counter counts from 0000 to 1001 and then resets. The output weights of flip-flops in these counters are in

accordance with
8421-code. For instance, at the end of the seventh clock pulse, the counter output will be 0111, which
is the binary equivalent of decimal 7. In other words, different counter states in this counter are
binary equivalents of the decimal numbers 0 to 9. These are different from other decade counters
that provide the same count by using some kind of forced feedback to skip six of the natural binary
counts.
2M
circuit diagram (can b using 74161 IC or it can b using 4 D flip flop)
2M
Truth table
1M

c. Johnson Counter
Circuit diagram.

d. Bidirectional shift register

A bidirectional shift register allows shifting of data either to the left or to the right. This is made 1M
possible with the inclusion of some gating logic having a control input. The control input allows
shifting of data either to the left or to the right, depending upon its logic status

74194 IC is used as bidirectional shift register
2M
Diagram using Ic
Working of circuit 2M

e.

f. Design ripple counter

Explain design procedure

1. Determine number of flip flop required.(3 flip flop)
2. Draw the state transition diagram.(111 110 101 100 011) 1M
3. Write excitation table for the counter, listing the present states, the next states 2M corresponding to the present states and the required logic status of the flip-flop inputs (the J and K inputs if the counter is to be implemented with *J-K* flip-flops).
4. Draw the circuit diagram
   2M
